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All-Silicon IQ Modulator for 100 GBaud 32QAM Transmissions

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Abstract: We experimentally demonstrate an all-silicon modulator operating at 100 Gbaud 32QAM. We achieve BER below the 20% FEC-threshold for a line-rate of 500 Gb/s on a single polarization. We describe signal processing and chip operating point optimization.
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1. Introduction

Photonic integration of high-speed single-carrier transceivers is a key enabler for future DWDM systems, offering advantages of smaller form factor, and lower cost and power consumption. Most commercial single-carrier 400G/600G systems run at 64 Gbaud with modulation formats of 16/64QAM. Scaling to single carrier 800G or 1T for optical interfaces will require higher-order QAM running at 100 Gbaud and beyond [1, 2]. In [3], an InP-based transmitter running at up to 100 Gbaud 32QAM is reported. Silicon photonics is less explored than InP for high baud-rate systems, despite advantages of large-wafer manufacturing and on-chip polarization manipulation. In [4], 100 Gbaud 16QAM was demonstrated using silicon organic hybrid (SOH) technology. However, incorporating SOH into a standard CMOS-compatible silicon photonics process is not trivial. A depletion-mode all-silicon solution, on the other hand, can achieve large-scale photonic integration using a CMOS-compatible silicon photonics foundry processes. Nevertheless, it is more challenging to achieve a high-quality QAM signal using a depletion-mode silicon modulator for 100 Gbaud and beyond due to the physical limitations on modulation efficiency and bandwidth. To date, the highest baud rates demonstrated with an all-silicon modulator are 85 Gbaud 16QAM and 64 Gbaud 64QAM [5], and 72 Gbaud 32QAM [6]. For 100 Gbaud operation, all-silicon based QAM generation has yet to be reported.

We demonstrate a depletion mode all-silicon modulator operating at 100 Gbaud and 32QAM, corresponding to a line-rate of 500 Gb/s on a single polarization. Several system operating parameters and reception algorithms were optimized, including diode bias voltage, digital and optical pre-compensation, and receiver side digital signal processing. The generated single-polarization 100 Gbaud 32QAM signal achieved bit error rate (BER) at 1.3e-2, below the 20% forward error correction (FEC) threshold, for a net rate of 416.7 Gb/s on a single polarization. To the best of our knowledge, this is the first demonstration of 100 GBaud QAM generation using an all-silicon modulator.

2. Signal Processing and Experimental Setup

Our depletion-mode silicon photonics (SiP) IQ modulator has two Mach-Zehnder modulators (MZMs) with traveling-wave electrodes applied. A laterally doped p-n junction in a 220-nm-high silicon rib waveguide is used as the phase shifter; design details can be found in [6]. The frequency response of the modulator varies with bias voltage. The 3-dB bandwidth is $\sim$ 24 GHz at zero bias, $\sim$ 32 GHz at -0.75 V, and $\sim$ 34 GHz at -3 V.

The experimental setup is shown in Fig. 1. A continuous wave carrier at 1530 nm with 100 kHz linewidth is provided by an external cavity laser (ECL). The carrier is boosted to 23 dBm by a high power erbium doped fiber amplifier (EDFA), and coupled to the silicon chip via a fiber array. The modulator is operated at the null point and probed with I and Q drive signals. A 50 GHz Keysight M8194A digital to analog converter (DAC) with 8 bit resolution was operated at 120 GSa/s to generate QAM signals. Data is prepared offline per the digital signal processing (DSP) flowchart in Fig. 1. A pseudo random binary sequence (PRBS) of order 19 is mapped to Grey-coded QAM symbols. A pre-equalization filter minimizing mean square error is applied to compensate for the DAC, cables and receiver front end. The QAM symbols are raised-cosine shaped with roll-off factor of 0.01. For each baud rate tested, the signal is re-sampled to match the DAC sampling rate, leading to various numbers of samples per symbol. After clipping and quantization, samples are loaded to the DAC. The outputs of the DAC are amplified by 50 GHz 18 dBm RF drivers.

A nonlinear predistortion method based on the iterative learning control (ILC) technique in [7] was used in quasi-real-time adaptation with hardware-in-the-loop. An optical filter provides additional pre-equalization; the digital and

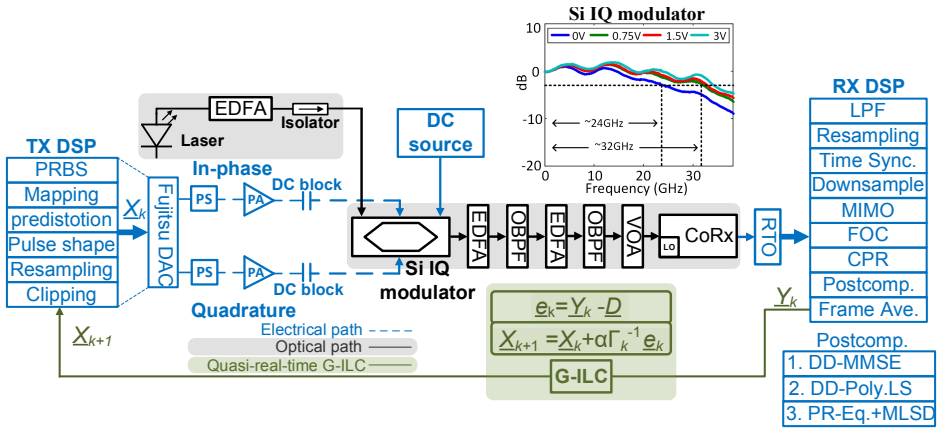


Fig. 1: Block diagram of DSP and experimental set-up; inset of modulator frequency response

optical pre-equalization were jointly optimized [6]. At the reciever side, DSP includes a 10^{th} order super Gaussian digital filter, resampling, T/2 spaced multi-modulus algorithm, frequency offset compensation (FOC), carrier phase recovery (CPR) by blind phase search, and a decision-directed minimum mean square error (DD-MMSE). To enhance post-compensation we cascade decision-directed memory polynomial least square (DD-Poly. LS) filters with 1st and 3rd order terms [9], and partial response equalization via a maximum likelihood sequence detector (MLSD) [8].

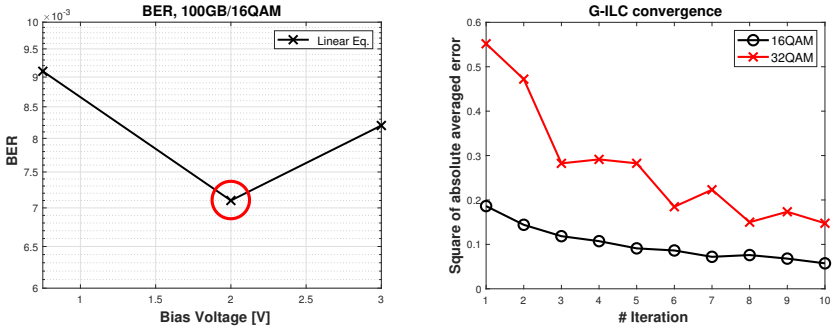
The modulated chip output is amplified by a two stage EDFA to compensate for coupling loss. On-chip insertion loss of the IQ modulator is measured to be 6.8 dB. The coupling loss from a fiber array to the I/O grating couplers on the SiP die was 8.5 dB. A programmable optical filter (Finisar Waveshaper) is placed after the MZM for optical-domain precompensation before transmission. Two optical bandpass filters (OBPF) suppress out-of-band amplified spontaneous emission (ASE) noise. We use a variable optical attenuator (VOA) to sweep received optical power. A discrete coherent receiver (CoRx) with 70 GHz bandwidth and a local oscillator (LO) with 16.5 dBm power are used for reception. Electrical outputs are digitized by a 160 GSa/s, 60 GHz, real-time oscilloscope (RTO) from Keysight.

3. Results and discussion

Due to the physical limitation of our designed silicon IQ modulator, which has a bandwidth of ∼35GHz with V_π around 6.5V, the operation of 100 Gbaud signal generation requires an overall optimization through electrical, digital and optical equalization. The DC bias voltage affects both V_π and modulator bandwidth for a depletion-mode SiP modulator. Higher DC bias increases the modulator bandwidth, but sacrifices V_π, lowering modulation efficiency leading to higher modulation loss. Our previous demonstrations favored OSNR and sacrificed bandwidth. In this demonstration we are able to push baud rate at the expense of OSNR. Fig.2a shows the 100 Gbaud 16QAM BER dependence against DC-bias voltage using only linear equalizers. Unlike 60 to 80 Gbaud operation [6], 2V bias indicates the best trade-off for 100 Gbaud signaling. The optimization of system signal processing (both at transmitter, optical channel and receiver) enhanced performance and allowed achievement of record transmission rates. This demonstration highlights the full bandwidth achievable in a depletion-mode all silicon modulator.

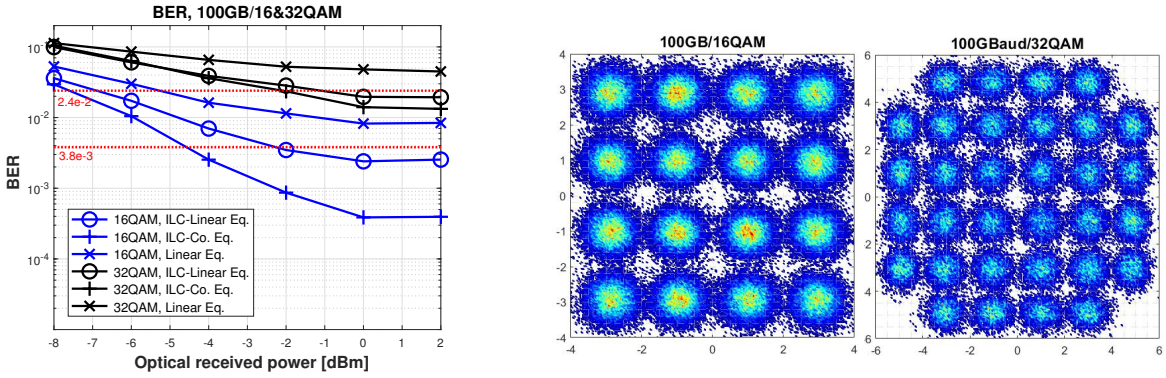
The remaining optimization can be classified into linear and nonlinear, with digital and optical filters. The linear part is conducted by jointly applying optical pre-compensation filter with different depths and further combine with a digital MMSE pre-compensation. The best combination is with 12dB pre-compensation for 100Gbaud signals. The nonlinear optimization is used at both transmitter receiver side DSP. At Tx, we use an adaptive ILC based pre-distortion to overcome pattern related distortion from DAC, driver and silicon modulator. Convergence is shown in Fig. 2b. The post nonlinear equalizers at Rx include 3rd order correction and partial response correction. The optimized BER results in Fig. 3a combine the best linear compensation with different nonlinear compensation filters for 16QAM and 32QAM.

The black curve marked with cross shows the 100 GBaud 16QAM BER performance with only linear pre- and post- compensation, reaches a BER floor above threshold of 7% FEC overhead. After applying ILC based non-linear correction, the performance can be improved to 1.7e-3 at 0dBm receiver power. In the post DSP part, adding polynomial based post-equalizer and MLSD detection give another boost, finally reaching the BER of 3.9e-4 at the 0dBm receiver power, well below 7% FEC threshold of 3.8e-3. The corresponding constellation after digital linear equalizer



(a) (b)

Fig. 2: a) BER sweep versus bias voltage b) Error sweep versus biteration number in G-ILC method



(a) (b)

Fig. 3: a) BER sweep of 16/32QAM at 100 GB using linear pre-equalizer and ILC at the transmitter side and DD-MMSE, DD-Poly-LS and MLSD at the reciever side, b) Constellation plots with

(DD-MMSE) is shown in Fig.3 b.

4. Conclusion

We have achieved 16QAM and 32QAM back-to-back transmissions at 100 Gbaud with a SiP IQ modulator for up to 416 Gb/s net rate per single polarisation. To the best of our knowledge, this is the first demonstration of 100 Gbaud QAM operation using an all-silicon modulator.

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